DIGITAL CPFSK TRANSMITTER AND NONCOHERENT RECEIVER/DEMODULATOR IMPLEMENTATION[1]

Eric S. Otto and Phillip L. De León
New Mexico State University
Center for Space Telemetry and Telecommunications

ABSTRACT

As radio frequency communications continue to grow, the available frequency spectrum becomes a valuable commodity, and as such may best be utilized in smaller and smaller increments. Hence, bandwidth efficient modulation schemes are desirable in that they allow better use of the frequency spectrum.

Previous research has considered the spectral efficiency characteristics of several modulation schemes. It can be shown that eight- and 16-level Continuous Phase Frequency Shift Keying (CPFSK) can achieve 2 bits/s/Hz spectral efficiency packing density with an E_b/N_0 of 12 dB specified at a 10^{-5} bit error rate [2]. In addition to its spectral characteristics, CPFSK possesses two other appealing characteristics. First, CPFSK maintains a constant amplitude signal, which is appropriate for nonlinear channels, as it will experience fewer adverse effects than a non-constant envelope signal. Hence, a non-linear high power amplifier in the signal path is acceptable. Second, the information in a CPFSK signal can be retrieved via non-coherent demodulation, which is appropriate for multipath fading channels.

This paper describes a low cost implementation of a CPFSK transmitter and noncoherent receiver based around the Motorola DSP56002 (56K) digital signal processor. In addition to the features associated with CPFSK, this implementation requires little power and is physically small and thus is suitable for many telemetry applications.

1. INTRODUCTION

This project describes an implementation of a continuous phase frequency shift keying (CPFSK) transmitter and receiver pair. This project has been driven by the need for bandwidth efficient modulation schemes in telemetry applications on missile ranges. The current standard for missile range

[1] This work has been funded by the International Foundation for Telemetering

applications is a pulse coded modulation/frequency modulation (PCM/FM) system with discriminator detection [2]. This existing standard has a spectral efficiency packing density of 0.85 bit/s/Hz with a 13 dB E_b/N_0 signal-to-noise ratio (SNR) and will achieve a 10^{-5} bit error rate (BER). One defining parameter of the system is the modulation index, *h*, given as

$$h = 2 f_d T \qquad (1)$$

where f_d is the maximum single sided peak frequency deviation and *T* is the bit period. Hence, reducing *h* decreases bandwidth. The current system uses *h* = 0.7. This project reduces *h* to 0.2. Table 1 lists parameters of the CPFSK system implementation.

Table 1: Operating Parameters of CPFSK System

Parameter	Description	Value
f_s	Sampling Rate	9600 Hz
R_s	Data Rate	300 bps
f_c	Carrier Frequency	2400 Hz
T	Symbol Interval	32 samples
h	Modulation Index	0.2

2. DESCRIPTION OF THE CPFSK SIGNAL

The CPFSK signal is a special case of a phase (PM) modulated signal of the form [1]

$$\sqrt{\tfrac{2E}{T}} \cos(2\pi f_c t + \phi(t)) \qquad (2)$$

where *T* is the bit interval, *E* is the energy expended during the bit interval, f_c is the carrier frequency and $\phi(t)$ is the modulating phase term which is determined by the input data. The CPFSK signal is a special case of (2) as $\phi(t)$ is constrained to be continuous.

An *M*-ary system [1] has data symbols defined as α_i = {-(*M*-1), …, -3, -1, 1, 3, …, (*M*-1)} for $0 \le i \le M-1$. The phase contribution of the CPFSK signal is then described by

$$\phi(t,a) = 2\pi h \int_{-\infty}^{t} \sum_{i=-\infty}^{\infty} \alpha_i g(\tau - iT) d\tau \qquad (3)$$

where

.

$$g(t) = \begin{cases} \frac{1}{2T} & 0 \le t \le T \\ 0 & \text{elsewhere} \end{cases} \quad (4)$$

The complex baseband CPFSK signal is then

$$s_l(t) = e^{j\phi(t,a)} \quad (5)$$

and the transmitted, frequency shifted version will be

$$s(t) = \sqrt{\tfrac{2E}{T}} \cos(2\pi f_c t + \phi(t,a)) \quad (6)$$

where only the real part of the signal need be sent as the imaginary part can be obtained using an in-phase and quadrature (I-Q) demodulator. Equation (6) is equivalent to

$$\sqrt{\tfrac{2E}{T}} \cos(2\pi(f_c \pm f_d)t)\,. \quad (7)$$

3. CREATING THE CPFSK SIGNAL

To efficiently generate sinusoids using the DSP, sampled sinusoidal values are stored in memory in a sine-lookup table. The DSP56K comes with an on-chip ROM containing N = 256 samples of a single sine wave period [3]. These samples are defined by

$$S(i) = \sin(i \tfrac{360}{N}) \quad (8)$$

for $0 \le i \le N-1$, where i is the index into the sine-lookup table.

The sine-lookup table allows the programmer to create low-distortion sinusoids of variable frequency in real time. The frequency of the sinusoid generated is a function of the sampling rate and the phase angle increment (Δ) between successive sine-lookup table accesses. By choosing appropriate values of Δ, one can efficiently generate the signal described by (7) [3]. Note that (7) maintains two unique transmitted frequencies by virtue of the square pulse shaping function used; therefore, only two unique values of Δ are required in order to generate the CPFSK frequencies.

4. RETRIEVING THE TRANSMITTED DATA

Once the data has been encoded, modulated and transmitted, there must be a way to retrieve the original data. The receiver was implemented in three parts: a demodulator, correlation filters and a decision algorithm. The demodulator returns the real transmitted signal to a complex baseband signal. Complex correlation is then done between the signal received and the two possible signals sent. The correlators output four scalar values, which are the real and imaginary parts of the received signal correlated with the possible signals sent. The decision algorithm then operates on the current correlator outputs, as well as the two previous bit periods' correlator outputs, and makes a decision on the middle bit under observation.

Since only the real part of the complex signal has been sent, an I-Q type demodulator, shown in Figure 1, is used to return the received and sampled signal, *r(n)*, to baseband and obtain the real and imaginary parts of the transmitted information bearing signal.

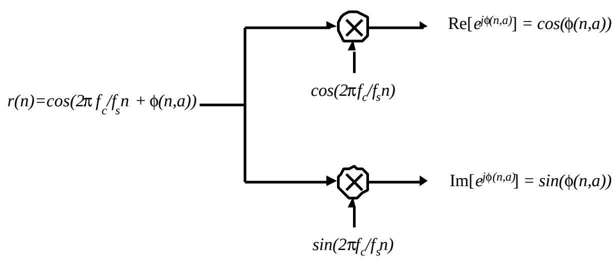

Figure 1: I-Q Demodulator

where $n = 1, 2, \ldots, kN$, with k representing the number of bits sent and N the number of samples per bit.

Once the signal has been returned to baseband, correlator receivers are used to determine the components of the signal sent with respect to each of the possible signals sent. From these values, a decision algorithm will make the best estimate of the data symbol sent based on a maximum likelihood block estimate [4]. From the CPFSK definition, the signal sent will be

$$s_l(t) = e^{j\pi h\alpha_i \frac{t}{T}}. \qquad (9)$$

Complex correlation requires that the conjugate of the signal sent be used as the correlating signal for optimum reception. Thus, there are two correlators, each matched to the conjugate of the possible signals sent. The output of the correlators is defined by

$$\mathrm{Z} = \int_0^T r_l(t) e^{-j\pi h\alpha \frac{t}{T}} dt \qquad (10)$$

where $0 \le t \le T$ and $r_l(t)$ is the received and demodulated complex baseband signal. Using Euler's identity, complex multiplication and the trigonometric identities cos*(-x)*=cos*(x)* and sin*(-x)*=-sin*(x)*, (10) can be expanded to create Figure 2.

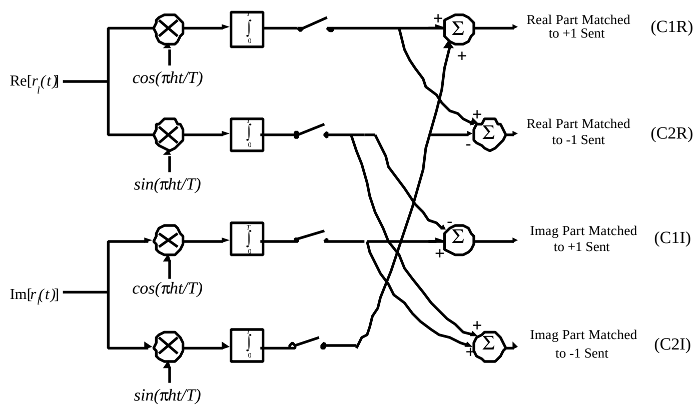

Figure 2: Theoretical Realization of Correlator Receiver

At the symbol time, T, each correlator output is integrated, sampled and recombined in such a fashion as to obtain the real and imaginary parts of the received signal correlated with each of the possible sent signals. Note that each of these outputs has been designated a variable, representing its time, correlator, and complex status.

While the system shown in Figure 2 is a continuous-time representation of the correlation and recombination process, a discrete-time equivalent is required. The four multiply and integrate operations in Figure 2 can be replaced by the four vector inner products described as

$$\begin{aligned} y_1(kN) &= \mathbf{R}_{kN}{}^{\mathrm{T}}\mathbf{x}_c \\ y_2(kN) &= \mathbf{R}_{kN}{}^{\mathrm{T}}\mathbf{x}_s \\ y_3(kN) &= \mathbf{I}_{kN}{}^{\mathrm{T}}\mathbf{x}_c \\ y_4(kN) &= \mathbf{I}_{kN}{}^{\mathrm{T}}\mathbf{x}_s \end{aligned} \qquad (11)$$

where

$$\begin{aligned} \mathbf{R}_{kN} &= [\mathrm{Re}[r(kN-0)]\ \mathrm{Re}[r(kN-1)] \cdots \mathrm{Re}[r(kN-N+1)]]^{\mathrm{T}} \\ \mathbf{I}_{kN} &= [\mathrm{Im}[r(kN-0)]\ \mathrm{Im}[r(kN-1)] \cdots \mathrm{Im}[r(kN-N+1)]]^{\mathrm{T}} \\ \mathbf{x}_c &= [\cos(\pi h \tfrac{0}{N})\ \cos(\pi h \tfrac{1}{N}) \cdots \cos(\pi h \tfrac{N-1}{N})]^{\mathrm{T}} \\ \mathbf{x}_s &= [\sin(\pi h \tfrac{0}{N})\ \sin(\pi h \tfrac{1}{N}) \cdots \sin(\pi h \tfrac{N-1}{N})\ ]^{\mathrm{T}} \end{aligned} \qquad (12)$$

where k represents the bit period under consideration.

When correlator outputs have been obtained for three bit periods, a metric must be calculated for each possible data vector sent in order to make a decision on the middle symbol. For each input data vector, [4] shows that the maximum likelihood block detection metric (for binary CPFSK and a three symbol observation interval) can be written as

$$\beta_{k,l,m} = A_k + e^{-j\pi h \alpha_k}[B_l + e^{-j\pi h \alpha_l} C_m] \qquad (13)$$

for k = 1, 2; l = 1, 2; m = 1, 2; and where A is the complex valued correlator output over the n–2[nd] bit interval, B is the complex valued correlator output over the n–1[st] bit interval and C is the complex valued correlator output over the n^{th} bit interval. The complex constants are phase contributions from each previous symbol. Hence, (13) calculates β for all possible data vectors. Finally, $\max[\left|\beta_{k,l,m}\right|^2]$ gives the most likely path and the middle bit is chosen accordingly.

A digital transmitter and receiver for the binary CPFSK with three symbol observation interval receiver have been designed and tested. However, before the system can be implemented to "real world" standards, there are some things to be considered.

Without considering initialization, the system implemented requires a total of approximately 307 words of program memory. The maximum number of instructions executed per sample period is approximately 1036. Since the 40 MIPS 56002 can perform more than 4000 instructions per sample at a 9600 Hz sampling rate, it can easily accommodate such a computational requirement. Finally, Matlab simulations show that reliable operation of the CPFSK system requires a minimum of four samples per symbol. Thus, in theory, an 8000 bps data rate with a 32000 Hz sampling rate yields four samples per symbol and would be the maximum data rate available for this system when using the 56002 at 40 MIPS. Higher sample rates and thus higher data rates could be accommodated on a similar DSP board.

The system described has been created using a three symbol observation interval receiver with a binary CPFSK signal. However, [2] determined that *4*-ary CPFSK signaling with five symbol observation performs much closer to the current standard with respect to BER performance. When considering an M-ary system with L symbol observation, the number of decision variables (β) to be considered is M^L. By knowing the number of multiplications necessary for the decision algorithm, x, one can derive an equation that determines the approximate necessary computational power of the DSP to be used to determine all values of β as

$$p_{DSP} = R_s M^L x \;\; \left(\tfrac{\text{instructions}}{\text{second}}\right). \qquad (14)$$

Hence, as M, L and R_s get large, the required computational power of the DSP grows very quickly, and as such, the required computational power should be thoroughly investigated before implementation of a higher level CPFSK system in the digital domain is considered.

Another consideration of the system is the multipath fading issue. This system has been considered for further study due to its supposed desirable characteristics under such conditions. However, while the multiple symbol observation system performs well in noisy conditions, a single symbol receiver performs better under multipath fading conditions [2]. It may therefore be desired to investigate schemes to bolster the performance of the multiple symbol observation interval receiver.

5. BIT ERROR RATE PERFORMANCE RESULTS

Figure 3 shows the results of the CPFSK binary system with respect to a Matlab simulation with identical parameters. Noise introduced to the signal is additive white Gaussian noise. Figure 3 shows agreement between the 56K implementation of the CPFSK system and simulation results from Matlab. Low BER values were not accurately obtained due to the length of data sets required. However, BER results at lower SNRs follow theory closely and give no indication that BER performance will deviate at higher SNRs.

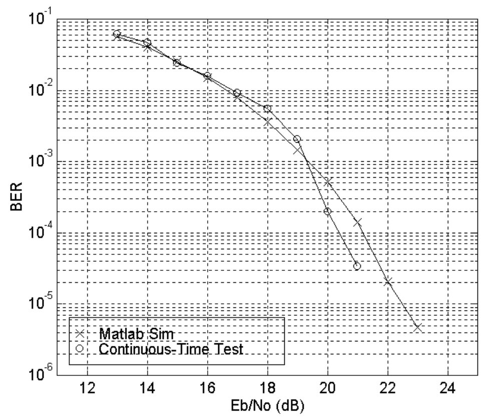

Figure 3: BER Performance of 56K Implementation of CPFSK System vs. Matlab Simulation

6. CONCLUSIONS

This paper has documented the implementation of a DSP-based system for CPFSK transmission and reception. Furthermore, the DSP system used requires little power and is cost-effective. BER results of the system were reliable with respect to theory and simulations. While higher data rates are possible using the same DSP system, higher powered processors will accommodate even higher data rates. Finally, concerns regarding multipath fading and higher order implementations remain, and are candidates for further research.

REFERENCES

[1] Anderson J., Aulin T., and Sundberg C.-E., *Digital Phase Modulation,* Plenum Press, New York, 1986.

[2] Ara, S. and Horan, S. B., "Development of a New Modulation Standard for Telemetry Systems," *NMSU Klipsch School of Electrical and Computer Engineering Technical Report Series, Dec. 1996.*

[3] Motorola, "Sine Wave Synthesis with the DSP56001/2," 1992

[4] Simon, M.K. and Divsilar, D., “Maximum-likelihood Block Detection of Noncoherent Continuous Phase Modulation,” *IEEE Transactions on Communications*, Jan. 1993.